Modified Low Power Binary to Excess Code Converter

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Abstract

Utilization of power is a major aspect in the design of integrated circuits. Since, adders are mostly employed in these circuits, we should design them effectively. Here, we propose an easy and effective method in decreasing the maximum consumption of power. Carry Select Adder is the one which is dependent on the design of two adders. We present a high performance low-power adder that is implemented. Also, here in Carry Select Adder, Binary Excess Code-1is replaced by Ripple Carry Adder. After analyzing the results, we can come to a conclusion that the architecture which is proposed will have better results in terms of consumption of power compared to conventional techniques.
Keywords: *Carry Select Adder (CSLA), Ripple Carry Adder (RCA), Binary Excess Code-1, low power.*

I. Introduction

Adders are mainly used in networking and DSP oriented system and they are also integrated in the calculators. The objective of a good adder is to consume low power. The important key factor of this work is that to improvise consumption of power by employing the converters like binary to excess-1. BEC functionalities and its architecture are discussed in detail in the second part. The rapid adder is the Carry Select Adder. It contains a multiplexer, two Ripple Carry Adders which will be discussed later. Apart from that, zero input is given for one Ripple Carry Adder and the other is given by input one. RCA with the input one is replaced by Binary excess Code-1[2]. The carry which is propagating acts as a selection input for the multiplexer.

II. Related Work

Conditional sum adder has a Carry Select Adder which is shown in below figure. In general, it has a multiplexer, two Ripple Carry Adders. So, to evaluate two times, we are going to use two n-bit numbers which are added to Carry-Select Adder. Here, once we go for approximating the carry to zero, another carry to one. Thereafter calculating the results, we go for choosing a multiplexer if we aware of the correct carry. The output of the carry is then evaluated finally. Also, selection is carried out by a multiplexer and is shown in figure 1.

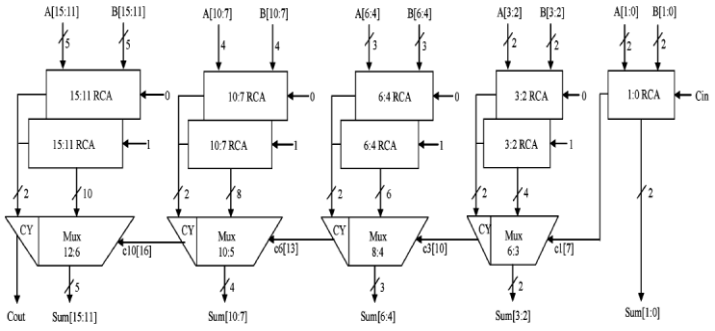

Fig 1: Carry Select Adder

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Multiplexer Selects partial sum based on Cin, and puts it in the result. The carry corresponding to the sum becomes Cout . Here, we generate a circuit by employing many full adders to add on N-bit numbers. Ripple Carry Adder is a circuit which is quite simple which generates addition of two numbers in the binary form. If every carrier ripples to the next level of full adder, then it is known as Ripple-Carry Adder. It consists of full adders which are attached end to end as a chain. Below figure shows the cascaded full adders which generates 4-bit ripple carry adder. Since the first term represents LSB, input is considered from right hand side. Also, in the below figure, cells a0 and b0 are the LSBs that are to be added. The sum is generated in the bits s0 – s3. Delays generated are the key issues to construct output carry signal and MSBs. Also, increments the various bits that are to be added. This is shown in figure 2 and 3 respectively.

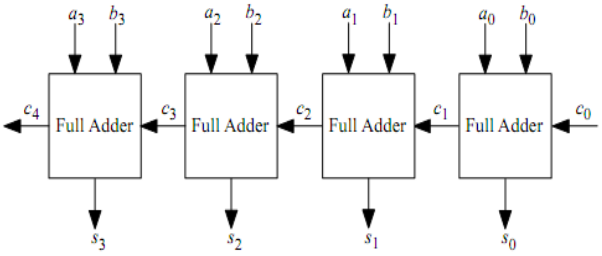

Fig 2: Schematic representation of Ripple Carry Adder

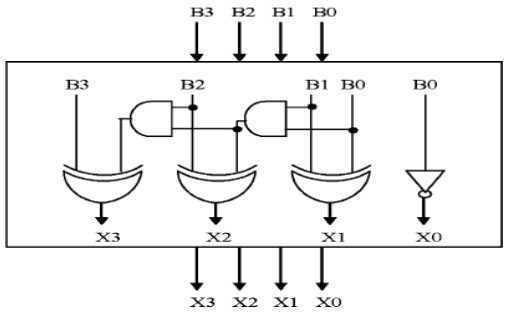

Fig 3: Schematic representation of Binary Excess Code

III. PROPOSED MODIFIED BINARY EXCESS CODE-1

The modified BEC consists of a NOT gate, AND gate and a multiplexer. Let's consider the example: 0001. From the Figure:4 we can see that the 0th bit (LSB) of a four bit code is a NOT gate input and one is the resultant output. In the next stage the 1st bit is given as an input to the NOT gate combined with the multiplexer. One of the inputs to the multiplexer will be one and the other input to the multiplexer will be zero. The 0th bit of the input is a selection line of the multiplexer, and the output will be one. The 0th bit and the 1st bit is AND gate input and resultant line acts as a selection line for the next stage of the multiplexer. The same process is repeated in the further stages. Hence the final output is 0010. So for a binary value 0001 the output is 0010.

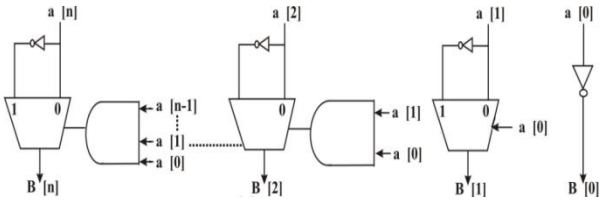

Fig 4: Modified Binary Excess Code-1

Above figure says that the CSA naturally contains Binary Excess Code, Ripple Carry Adder, multiplexer. Two n-bit numbers can be added knowing that zero carry and other to be one. BEC employs carry to be one. Hence, correct sum, carry are identified with a multiplexer if the known carry is correct. The output carry evaluated at the final stage says that the LSB is employed to choose calibrated values of carry, sum at the output. Selection is always ended by employing a MUX and is shown in figure 5.

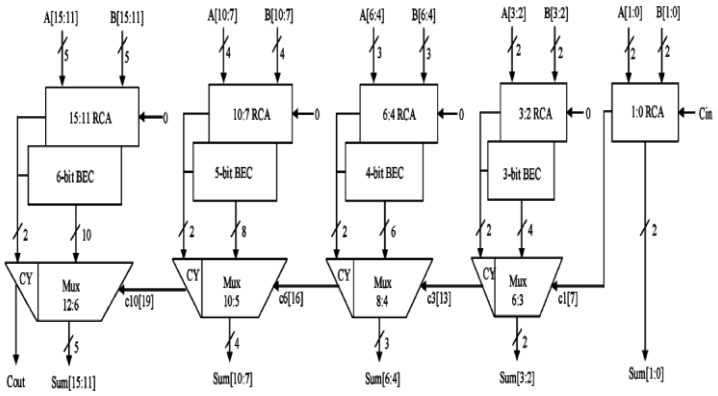

Fig 5: Schematic representation of Modified Carry Select Adder

The 5 bit BEC does the operation of adding one and it consist of AND gate, NOT gate and one multiplexer. Similarly the 4 bit BEC and 5 bit BEC have the gates and multiplexers accordingly. This is shown in figure 6.

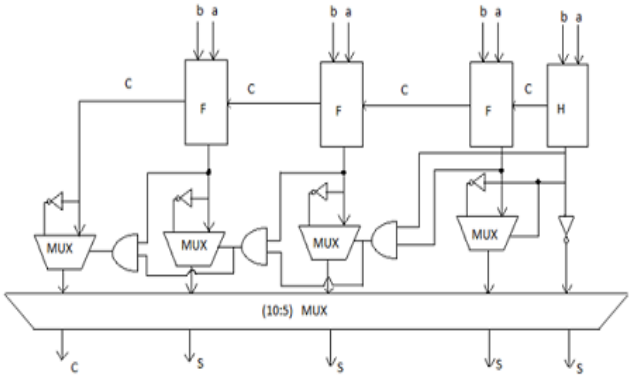

Fig 6: Schematic representation of (5-bit BEC)

IV. SIMULATION RESULTS

The design proposed in this paper has been developed using Verilog Hardware Description Language (VHDL) and synthesized in Xilinx, it can be implemented in Field Programmable Gate Array (FPGA). Carry Select Adder contains Binary Excess Code rather than Ripple Carry Adder that has a carry at the input is observed in the below figure. Let's consider the example: 0001. From the Figure:3 We can see that the 0th bit (LSB) of a four bit code is a NOT gate input and one is the resultant output. In the next stage the 0th bit and the 1st bit are given as input to XOR gate. Since the inputs are 0 and 1, the output of XOR gate is one. In the next stage one of the inputs is the multiplication of the 0th bit and 1st bit. And the other input is 2nd bit. Since the inputs are 0 and 0, the output of XOR gate is zero. The same process is repeated in the next stage with one of the input as 3rd bit. Hence the final output of 0001 is 0010. So when a binary value 0001 is given the output is 0010. Simulation analysis are shown in figure 6 and figure 7 respectively.

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Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	24	13,824	1%	
Number of 4 input LUTs	50	13,824	1%	
Logic Distribution				
Number of occupied Slices	27	6,912	1%	
Number of Slices containing only related logic	27	27	100%	
Number of Slices containing unrelated logic	0	27	0%	
Total Number of 4 input LUTs	50	13,824	1%	
Number of bonded IOBs	50	325	15%	
IOB Flip Flops	2			
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	508			
Additional JTAG gate count for IOBs	2,448			

Fig 6: Area notation of proposed converter

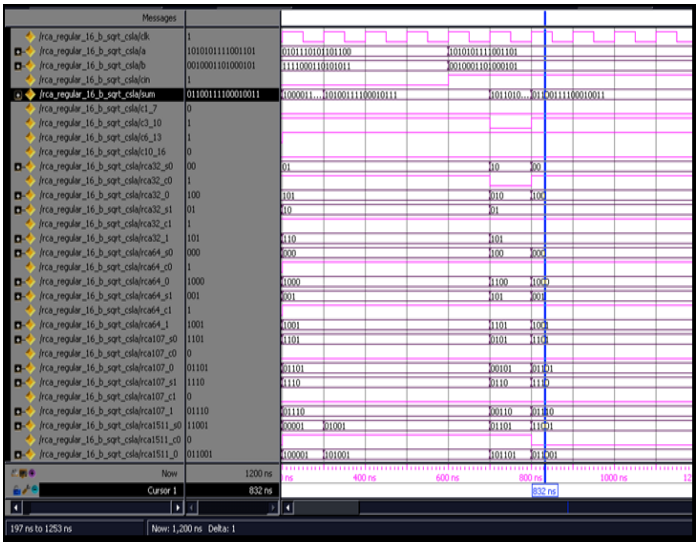

Fig 7: Simulation of binary to excess code converter

Table 1: Comparison Of The Binary Excess Code Results

Word Size	Adder	Area	Power(mw)
8 bit	Regular BEC	243	3344
8 bit	Modified BEC	237	3299
16 bit	Regular BEC	508	3227
16 bit	Modified BEC	502	3138

Below table 2 shows the differentiate between 4-bit Vedic ALU and array ALU in terms of their speeds. Simulation results show that array ALU less path delay in comparison with Vedic ALU. This 4-bit array ALU and it delay time will compared.

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V. Conclusion

The power consumed by adder using BEC is 0.89% reduced when compared to the power consumed by adder using regular BEC. The adders are designed using VHDL, Xilinx Project Navigator 8.1 is the synthesis tool that is adopted. Simulation is done on ModelSim 6.3. FPGA (Field Programmable Gate Array) Spartan 3 is used for implementing the designs.

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