Design and Analysis of Single Ended Low Noise Amplifier

Mrs. Monika Soni
Director, Auricle Technologies Bikaner Rajasthan India
editor@ijritcc.com

Article History

Article Submission
19 November 2014
Revised Submission
17 January 2015
Article Accepted
1 March 2015
Article Published
31st March 2015

Abstract

In this research article, we propose a Low Noise Amplifier which utilizes 1.748GHz (mid frequency) by employing 0.35µm CMOS technology. Gain of 33.25dB is obtained by using this technique and also having a noise figure of 2.233. Employing single ended configuration, we design a Low Noise Amplifier along with cascaded. The information transmitted can be either voice or data that alters radio frequency carrier from a transceiver in wireless communications.
Keywords: *LNA, CMOS ,NF*

I. Introduction

The information transmitted can be either voice or data that alters radio frequency carrier from a transceiver in wireless communications [1]. The first block of RF design is a LNA. Because of scaling, low cost, integral features, CMOS is becoming more and more powerful in different wireless communications for transceiver applications [2]. The main purpose in going for CMOS is its ease of installation on a single integrated chip. The major operation of low-noise amplifier to attain high gain to attack the noise in the next blocks. Attaining more gain with small noise, low-noise amplifier should hold many signals which are distortion free. Large dynamic range is offered by LNA. It also matches the input and output [3]. The main aspect is that it has a band select filter, prior image-reject filter. Finally, LNA depends on its noise figure and gain. LNA design is the one which has to provide minimum noise figure (NF) and satisfactory linearity. Apart from that, LNA employed in wireless communication system is having data rates which are low, power utilization is less where every node uses a voltage source. Therefore, here LNA is employed to achieve low utilization of power [4][4].

II. Related Work

Based on the way input matching is provided LNA can be classified into four architectures [6]. 1/gm or the common gate topology offers less gain and poor noise figure [7]. Common gate topology is popular for wideband designs gain can enhance through using gain boosting circuitry [8]. The circuit is shown in fig.1.

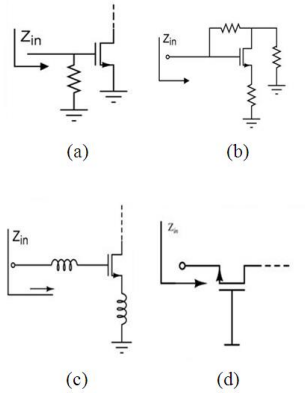

Fig 1: Circuit of Common LNA architecture (a) Resistive based Termination (b) shunt-series feedback (c) Inductive based source degeneration (d) 1/gm termination

ISSN: 2250-0839

Among all these inductive source degeneration has the lowest noise figure and it is very accepted for narrow band design [9]. As the system comes under narrow band applications we have selected inductive source degenerated LNA. It also has the advantage of high gain.

III. Proposed Lna Design Architecture

Low Noise Amplifier which utilizes 1.748GHz (mid frequency) by employing 0.35µm CMOS technology is implemented. It also uses single ended configuration. LNA specifically employs Advanced Design System. Below figure shows the schematic representation of LNA. Expressions for a LNA with single ended configuration can be seen below.

$$L_s = \frac{R_s}{\omega_T} = 0.48\text{nH} \qquad (1)$$

Here, Ls represents inductance of the source, Rs represents resistance of the source, cut off frequency is given by ω_T

$$C_{ox} = \frac{\mathcal{E}_{ox}}{T_{ox}} = 4.6\text{mF} \qquad (2)$$

$$\mathcal{E}_{ox} = \mathcal{E}_s.\mathcal{E}_o \qquad (3)$$

Here, C_{ox} represents capacitance, $\mathcal{E}_s$ represents silicon's dielectric constant, T_{ox} represents thickness of gate oxide. Also, transistor length is about 0.35 µm which is taken as minimum.

$$W = \frac{1}{{\omega_0}^2 L_{min} C_{ox} R_s} = 377\mu\text{m} \qquad (4)$$

Here, W represents transistor width, L_{min} represents length of the transistor which is minimum and ω_0 represents mid frequency.

Two N-MOS transistors are used in the design, the Transistor (M2) acts a biasing transistor and Transistor (M1) is the main transistor. Apart from above, M2 transistor width, R2 resistance value is maintained optimum for the gate voltage controlling of M1 transistor. LNA is specifically because of M1 transistor. Also, Resistance R2 has been chosen to provide as less noise as we can. There are two paths for RF signal to the ground. One is passed by C1,L1 and L2. The other one is passed by L1, R3 and L3. Impedance is very large in this circuit. The main purpose of R3 is to avoid capacitance from gate M2 to the ground. Now, the width and length of the transistors are given by 371µm and 0.35 µm respectively. Table 1 gives the important specifications.

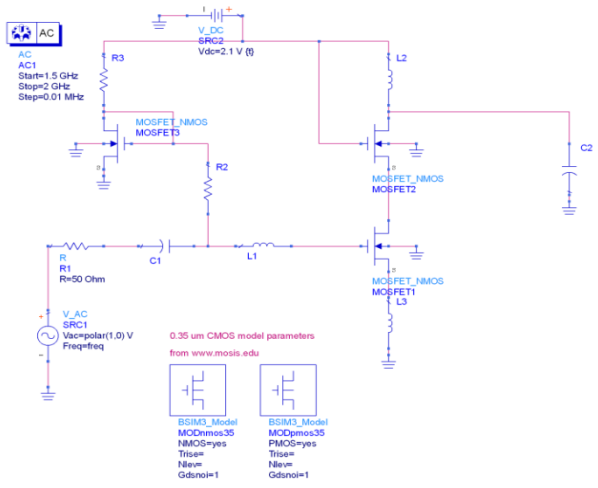

Fig 2: Schematic representation of Low Noise Amplifier Design

The important aspects of low-noise amplifier are mid frequency, length of the channel bandwith and transistor width.

TABLE 1: Design Specifications of Low Noise Amplifier

Parameter	Specification
Topology	Single ended LNA
Frequency	1800MHz
Center Frequency	1.748GHz
Channel Bandwidth	75 MHz
Channel length	0.35 µm
Width	377 µm
DC voltage	2.75V
Inductance	0.48nH
Oxide thickness	4.6mF
L_D	8.2nH

The main aspects of LNA are gain and Noise figure. Gain of LNA always more than 20dB and noise figure could be low as 2.5dB. Here, the implemented LNA attains a gain of 33.25 dB and a Noise Figure of 2.23. Expression for gain and Noise figure are given in equations (5) and (6) respectively.

Gain=20*log10 (Vout/Vin) (5)

Here, Vin represents voltage at the input and Vout represents voltage at the output.
Noise figure is a measurement of noise as frequency function. It is defined as the ratio of SNR and Radio Frequency signal.

NF= SNRi / SNRo (6)

Here, SNRi represents signal to noise ratio of LNA at the input and SNRo represents signal to noise ratio of LNA at the output.
The Low Noise amplifier is designed using single ended topology. The simulation is done using Advanced Design System software.

IV. Simulation Results

AC simulation is the one to attain Gain, Noise figure and SNR. At the implemented frequency, NF should be less Gain and SNR are made high. The simulation results are shown in figure 3(a)to 3(c).

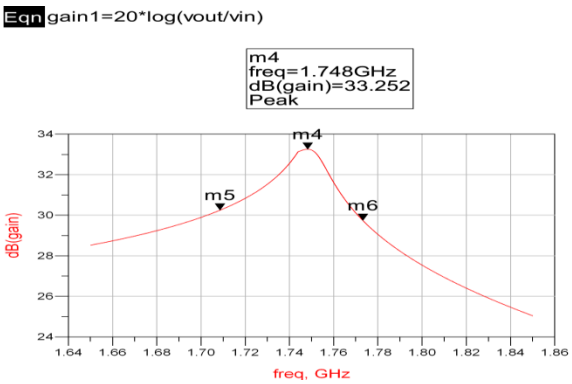

Fig 3(a): Simulation Graph representing Gain

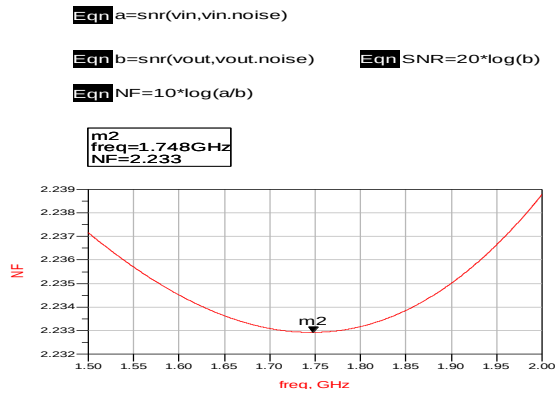

Fig 3(a): Simulation Graph representing NF

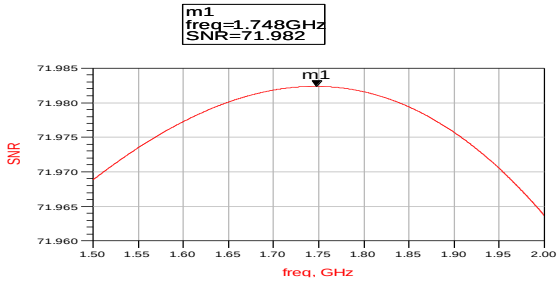

Fig 3(a): Simulation Graph representing LNA

Above figure represents, graphs of Gain, Noise Figure and SNR of LNA. It attains a gain of 32.35dB, Noise figure of 2.233, mid frequency is at 1.748GHz ,Signal to Noise ratio of 71. LNA design achieves in having high gain and noise figure which is less in the mid frequency.

Simulation of S-Parameter is obtained to loss return and stability factor. K>1 represents the circuit is stable unconditionally for the desired mid frequency. Expression for K is as follows.

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} \qquad (7)$$

Where $\Delta = |S11\ S22 - S12\ S21| < 1$

Here, the K>1, the circuit stable for all possibilities of source and load impedance. Simulations are shown in fig.4(a) to 4(c).

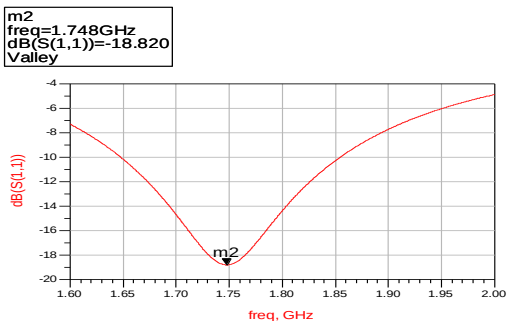

Fig 4(a): Simulation S parameter of LNA-Return loss (s11)

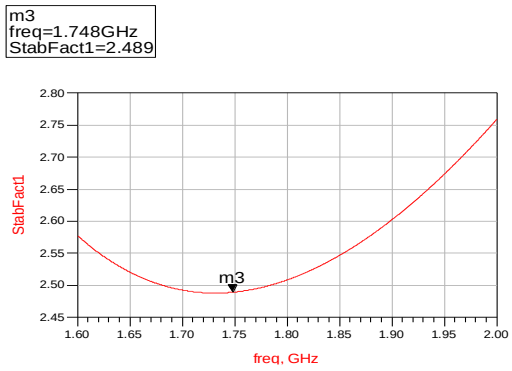

Fig 4(b): Simulation S parameter of stability factor (k)

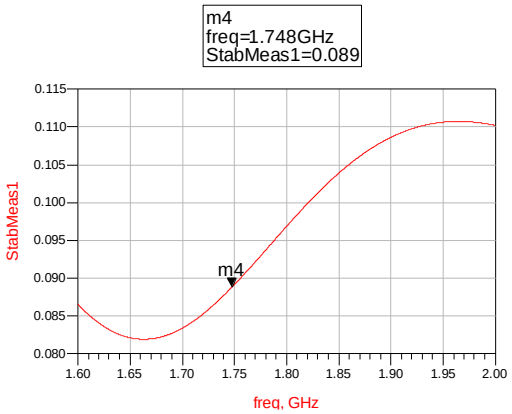

Fig 4(c): Simulation S parameter of Stability measure (Δ)

V. Conclusion

Designed return loss of LNA is given by -18.82dB, K=2.489 >1, Δ=0.089 <1. The above aspect says that the circuit is stable. Designed Low Noise Amplifier employing 0.35µm CMOS technology for mid frequency 1800Mhzis used in wireless communications receiver. It is simulated by employing Advanced Design System Software. The above results represents the circuit is stable unconditionally.

References

[1] Y. Imai, M. Tokumitsu, and A. Minakawa, "Design and performance of low current GaAs MMICs for L-band front-end applications," IEEE Transaction Microwave Theory Tech., vol. 39, pp. 209–215, Feb. 1991.

[2] J. Crols and M. Steyaert, "A single chip 900-MHz CMOS receiver front-end with a high -performance low-IF topology," IEEE Solid-State Circuits, vol. 30, pp. 1483–1492, Dec. 1995

[3] D. Shaeffer, T. Lee. —A 1.5 V, 1.5 GHz CMOS low noise amplifier, IEEE Journal of Solid State Circuits, Vol. 32, May 1997.

[4] S.Mahdavi and A. Abidi, "Fully integrated 2.2 mW CMOS front end for a 900 MHz wireless receiver," IEEE Journal on Solid-State Circuits, vol. 37, no.5, pp. 662–669, 2002.

[5] R. Montemayor and B. Razavi, "A self-calibrating 900-MHz CMOS image reject receiver," in Proc. 2000 Eur. Solid-State Circuits Conf., pp.292–295.

[6] D. Cordova, E. Fabris and S. Bampi, "A CMOS low noise trans conductance amplifier for 1–6 GHz bands," 2015 IEEE 6th Latin American Symposium on Circuits & Systems (LASCAS), Montevideo, 2015, pp. 1-4, doi: 10.1109/LASCAS.2015.7250452.

[7] M. Charchian, B. Zakeri and H. Miar-Naimi, "Wideband noise figure low noise amplifier design for 3.5–4.5 GHz," 2015 2nd International Conference on Knowledge-Based Engineering and Innovation (KBEI), Tehran, 2015, pp. 589-594, doi: 10.1109/KBEI.2015.7436111.

[8] C. J. Lee, H. J. Lee, J. G. Lee, T. H. Jang and C. S. Park, "A W-band CMOS low power wideband low noise amplifier with 22 dB gain and 3dB bandwidth of 20 GHz," 2015 Asia-Pacific Microwave Conference (APMC), Nanjing, 2015, pp. 1-3, doi: 10.1109/APMC.2015.7413040.

[9] M. Parvizi, K. Allidina and M. N. El-Gamal, "A Sub-mW, Ultra-Low-Voltage, Wideband Low-Noise Amplifier Design Technique," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 6, pp. 1111-1122, June 2015, doi: 10.1109/TVLSI.2014.2334642.

ISSN: 2250-0839