Power and Delay Analysis of Flip Flop Using Pulse Control Method

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Abstract		
The past few years, increasing difficulty in integration can be solved by low power,		
which is very important and also choosing flip-flop solves the challenges like low		
power. In this paper, we design and compare the power problem of various indirect		
pulse triggered flip flop are examined. It can be attained by reconstructing the lower		
part of Single-ended Conditional Capture Energy Recovery (SCCER) design and by		
employing the control pulse scheme. The results after the simulation derives		
transistor count and power required are significantly reduced in the proposed design		
over existing design.		
Keywords: flip flops, pulse, power, delay.		

I. Introduction

Single bit storage elements are known as flip flops. Flip flops are the heart of many digital electronic systems used worldwide. In the recent times, we are adopting flip-flop components in digital designs [1][2]. Utilization of power by storage components, clock is in between 20-45% of the whole set-up power. Consumption of less power is an issue in electronic systems. When coming to performance of an electronic system, power dissipation should be very low and it is more important right now. To achieve this purpose, we are going for LPVLSI [3].

In recent VLSI, low power is becoming a crucial issue with the increasing integration complexity. There are two power dissipations, one is active and the later is passive. These two limits system MOS effect and system performance [4]. Processors having high performance face an important issue like high power utilization due to the presence of high frequencies of the clock system in the device. We are going to reduce the utilization of power of flip-flop and clock matrix, since clock system only utilizes 30-60% of the whole power of the device. It helps in protecting the battery life of a system or device [5].

Flip-flop is a basic memory element which stores single bit at a time. In a circuitry form, it is a bi-stable multivibrator. FF has a sequential logic circuitry in digital designs and it consists of two latches. Flip-flop utilizes more power in comparison with a latch because of fewer gates in a latch. In any digital system design, majorly we will concentrate on synchronous sketch in decreasing complexity of integration and an important opposition is to plot a DFF [6].

Here, we propose a P-FF plot using a limiting pulse technique and to keep up this attribute we are using three more transistors. The reduction in total layout will not be affected with the increase in transistor number [7].

II. Previous Works

Firstly we will analyze P-FF designs and then we go comparisons which is shown in the following figure. It contains indirect data and FF design. Latching data is done by I5 & I6, inside junction values are taken care by I7 & I8. Finally pulse generator will take control of I1-I3. Here, two issues will arise in this design due to N2 is ON, N3 is ON [8]. Firstly, When node x is release due to '1' which leads to more power dissipation. In the other case, node x

takes authority over big transistors. At last, utilization of power is more in between heavy capacitive component and node x.

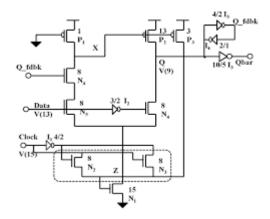


Figure 1: Structure of IP – DCO

Below figure shows MHLFF which is an upgrade of P-FF, which is presented in[10]. Here, the clock system does not helps in charging the node earlier. The FF result information Q, takes authority over P1. Q preserves the node to be '1' when it is '0', which reduces more utilization of power at the node. Meanwhile zero to one transformation, it keep up large information. MHLFF has two disadvantages, one is it experiences long information and the second one is that point converts to floating, if Q and information at the are '1'. Hence, it gives a wonderful enhancement in the reduction of transistors, spatial and power utilization [9].

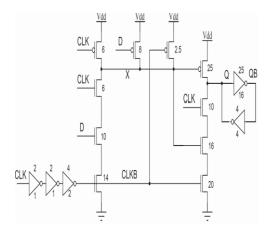


Figure 2: Structure of MHLFF

The figure shows SCCER, a kind of P-FF employing conditional discharged method. Here, P1 is placed instead of I7 and I8 with I2 to minimize the heavy capacitance. The dissipation way travels from N2 to N1 and N3(where Q has the authority). Therefore, if the information at the input is '1', then no power dissipation happens. If the information at the input is '1' and when the path is from N1 to N4, worst scenario in timing happen. So, we require a strong pull-down circuitry [10].

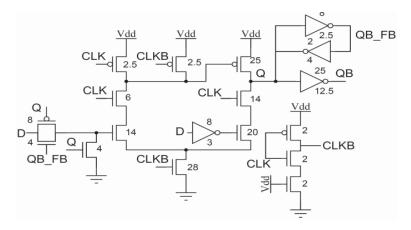


Figure 3: Structure of SCCER

III. Proposed Work

In this proposed design, disadvantages of P-FF designs are eliminated by using two different methods. In the first case, transistors count used is decreased. Whereas in the other case, requires a strong pull-down circuitry. In the above figures, in the dissipation path, N2 is released, and added with N3 to develop a PTL AND gate. Since from the figure AND inputs are opposite, node z is zero always. When AND logic inputs are zero, node z is safe. But at edges, when node z is high, N2and N3 transfers zero to node z. if the voltage is in the decreasing mode, this switching of node z is decreased. When compared to MHLFF, two transistors increases the logical functioning of the pulse that is produced. Also, Q is zero when the information at the input is one is the output in the dissipation path.

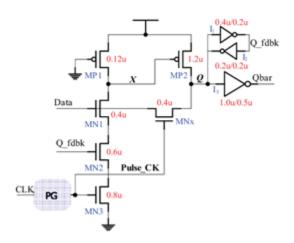


Figure 4: Structure of proposed flip flop

So, in this case P3 is conjucted and it is generally in OFF state when node x is '1'. This helps to node z and improved strong pull-down transistor N1 and vice-versa. Including P3, pulse width is increased add up to utilization of power in the produced pulse logic. This modifies the output Q and helps in good power utilization. Subsequently there is power leakage in the circuitry path.

IV. Simulation Results

To analyze the execution of pulsed flip flop, they are designed using Tanner S-EDIT Tool and the design structures are simulated using T-SPICE. All the schematics are based on the 180nm model files under a standard voltage of 5V, and operating frequency of 62MHz. The design and simulation results of the various flip flops and the proposed flip flops are shown below.

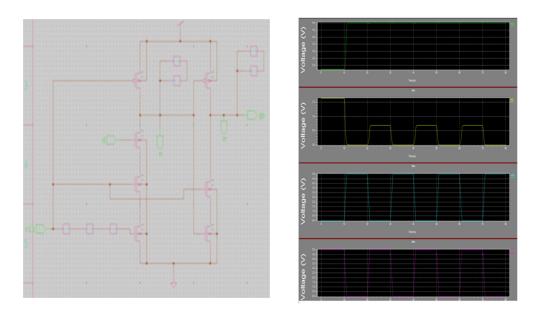


Figure 5: Schematic and waveform of ip-DCO

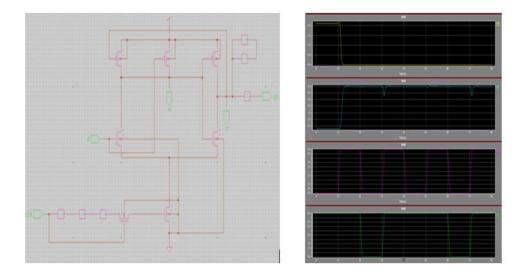


Figure 6: Schematic and waveform of MHLFF

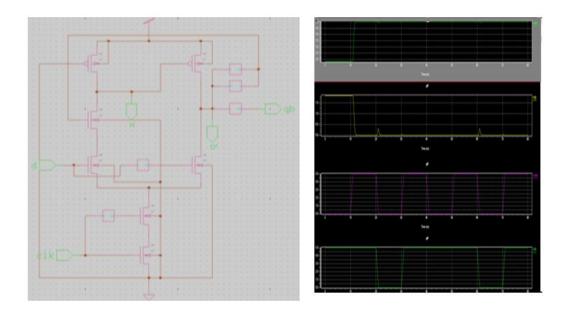


Figure 7: Schematic and waveform of SCCER

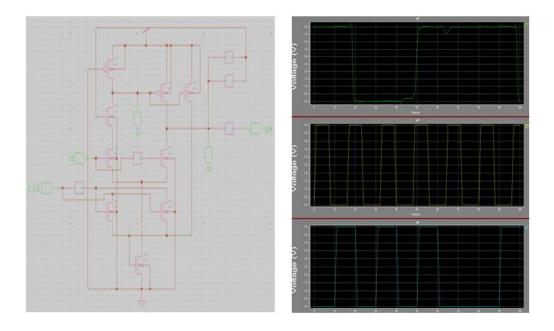


Figure 10: : Schematic & waveform P-FF using Pulse Control Scheme

Proposed flip flop is analyzed to compare among the performance metric parameters of various flip flops are done. From this comparison results the proposed P-FF employing pulse control method performed in a better way rather than conventional designs. The simulation results are tabulated in table 1.

Table 1: Performance analysis and Comparison of different types of FFs

PARAMETERS	Ip-DCO	MHLFF	SCCER	PROPOSED P-FF
Transistors count	24	19	18	19
Average power in (nW)	12.406452e-004	11.770468e-004	10.270526e-004	5.840202 e-004
Optimal PDP (fJ)	3.22	3.89	2.19	1.65

V. Conclusion

In this proposed, different methods are known and waveforms are identified. The table shown is used to compare different schemes. Simulation results make us to understand about various designs in knowing power utilization, transistor count. Also the discharging operation is achieved faster when needed in comparison with P-FF. The analysis result shows 60% improvement in area compared to conventional methods. The results also show 45% and 60% improvement in average power consumption and PDP respectively compared to MHLFF, SCCER and IP-DCO flip flops.

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