Design and Analysis of Low Power Energy Efficient Braun Multiplier

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Abstract

Designing of Braun multipliers using various hybrid full adder circuits are described in this paper. In DSP and communication systems, multipliers are the main power consuming elements. Dynamic power dissipation contributes a lot to power consumption in CMOS logic. Braun multipliers employing Row bypassing techniques are designed to minimise the switching activities which aids in reducing dynamic power consumption. Full adders constitute a most vital part in multipliers. In this paper, Braun multiplier is designed using three different hybrid full adders .Area and power consumption of the resulting circuits are compared and analysed. The Braun multipliers are implemented and simulated using Tanner spice.
Keywords*: Conventional Braun multiplier, Full adder, Carry save adder****.***

I. Introduction

Multiplication act as vital task in ALU unit and control the finishing time of almost all DSP algorithms. Instruction cycle of a Digital Signal Processing chip is mainly determined by multiplication time. A digital multiplier circuit multiplies an N bit multiplicand to N bit binary multiplier. A digital multiplier consists of a plurality of AND gates. These AND gates are used to multiply each digit of multiplicand to each digit of the multiplier and outputs of the AND gates represent the partial products that are then arranged corresponding to each digit of the multiplier. The multiplier also contains a plurality of 1's counter to receive all the partial products in parallel except the least significant digit of the multiplier. The most important type of the multiplier is parallel multiplier which is used to carry away elevated speed mathematical actions. Power consumption plays a vital role in the performance of these circuits [1]. So Braun multipliers employing row bypassing technique is used in order to decrease the dynamic power consumption. Full adders in this Braun multiplier are replaced by Radha Krishnan adder, Chang adder, Agarwal adder and their area and power consumption are compared and analyzed.

II. Conventional Braun Multiplier

This multiplier is termed as carry save array multiplier which performs multiplication of two unsigned bits. An nXn Braun multiplier necessitates nX(n-1) adders and n^2 AND gates. Products can be generated parallel using the AND gates. The partial product can be added to the computation of partial product that is formed by the lineup of adders. The carry out is shifted one bit to the left side or right side. Further, it will be summated to the sum that is produced by the 1st adder and the newly spawned partial product. The shifting would happen because of Carry save adder and the ripple carry adder is employed for the final stage output [2].

Mathematical analysis [4]:
Consider a generic mXn multiplication of two un-signed n-bit numbers $Y=Y_m\text{-}1\ldots Y_0$ and $X=X_n\text{-}1\ldots X_0$.

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$$Y = \sum_{i=0}^{m-1} Y_i 2^i$$

$$X = \sum_{i=0}^{n-1} X_i 2^i$$

The product P can be written as follows:

$$P = \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} (Y_i X_j) 2^{i+j}$$

			$A =$	a_3	a_2	a_1	a_0	
×			$B =$	b_3	b_2	b_1	b_0	
				a_3b_0	a_2b_0	a_1b_0	a_0b_0	
			a_3b_1	a_2b_1	a_1b_1	a_0b_1		
		a_3b_2	a_2b_2	a_1b_2	a_0b_2			
	a_3b_3	a_2b_3	a_1b_3	a_0b_3				
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	

Fig 1: Braun multiplication algorithm

Reduction of switching power consumption is achieved by row by-passing technique which immobilize the operation in selected rows [3]. The components used in braun multiplier with row bypassing are full adders, multiplexers, tri state buffer and AND gates. The multiplexer's select full adder output and by-pass signal. Tristate buffer serve as input gating when by-passing. For example if a bit b2 of figure is zero then the output from the second CSA are fed directly to fourth CSA row and the third CSA row is disabled which in turn reduces the power due to switching of third row. The addition function in the j^{th} row is disabled if the bit b_j in the multiplier is zero.

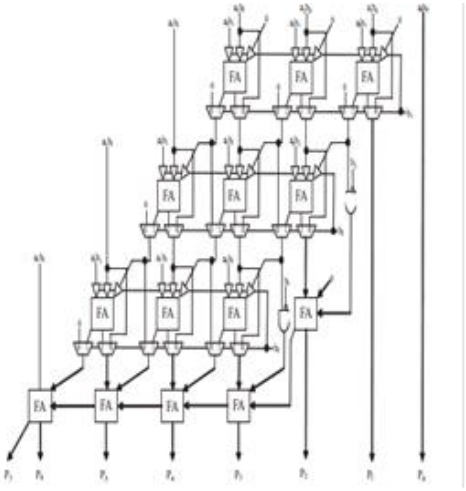

Fig 2 :Conventional Braun multiplier

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III. Proposed Braun Multiplier I

Proposed Braun Multiplier I has only six transistors for the XOR-XNOR cell. This leads to operational reliability when the supply voltage is scaled down. The total number of transistor for full adder is twenty two. [5] Using this adder circuit Braun multiplier is implemented.

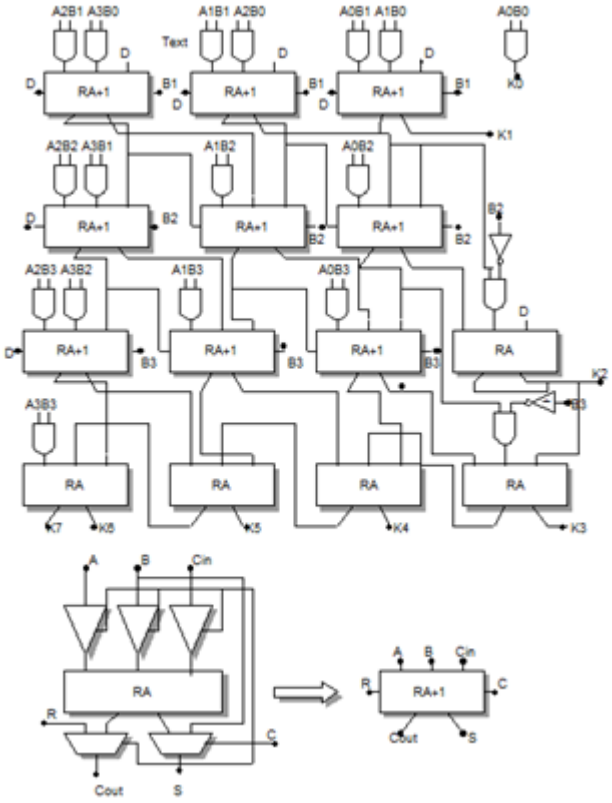
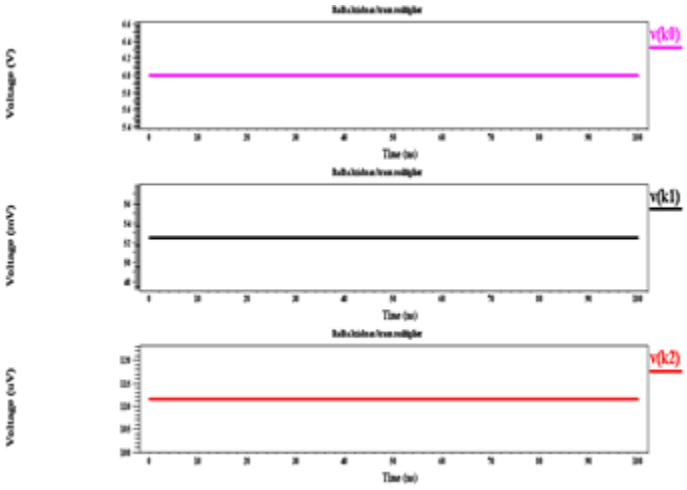


Fig 3: Proposed Braun multiplier I



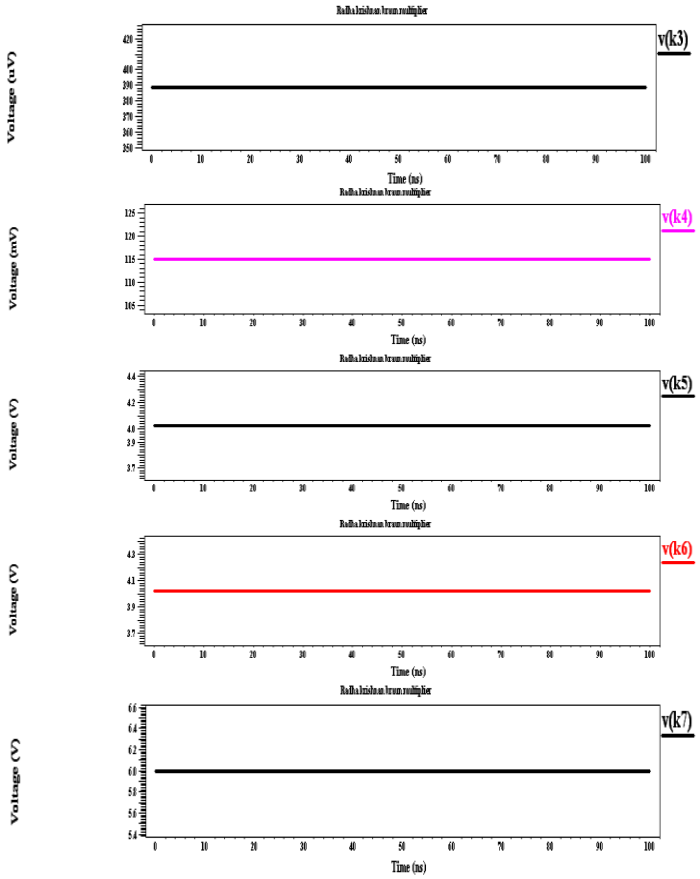


Fig 4: Waveform for Proposed Braun multiplier I

IV. Proposed Braun Multiplier II

Proposed Braun Multiplier II uses 26 transistors and it exploit a modified XOR/XNOR circuit. In the below circuit worst case delay harms because of less logical transitions due to adding up of more transistors. The extra transistors increase the power expenditure of the full adder cell [5]. Using this adder Braun multiplier is implemented.

V. Proposed Braun Multiplier III

Proposed Braun Multiplier III It uses CPL and this multiplier comprising of various adders is made by NMOS transistors and pull-up PMOS transistors to acquire full swing output voltage. Because of positive feedback and NMOS transistors, the circuit is intrinsically fast. This adder contains a well-balanced construction with esteem to generate sum and carry signals [5]. Using this adder Braun multiplier is implemented.

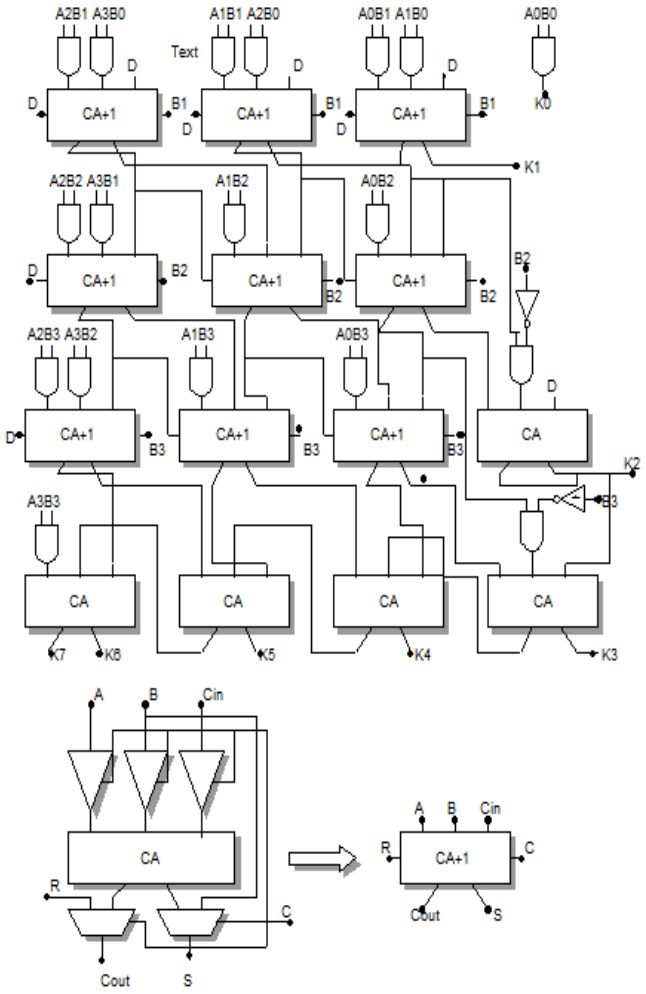
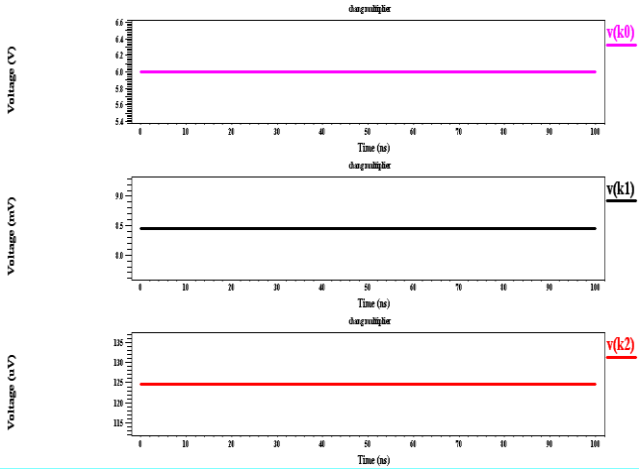


Fig 5: Proposed Braun multiplier II



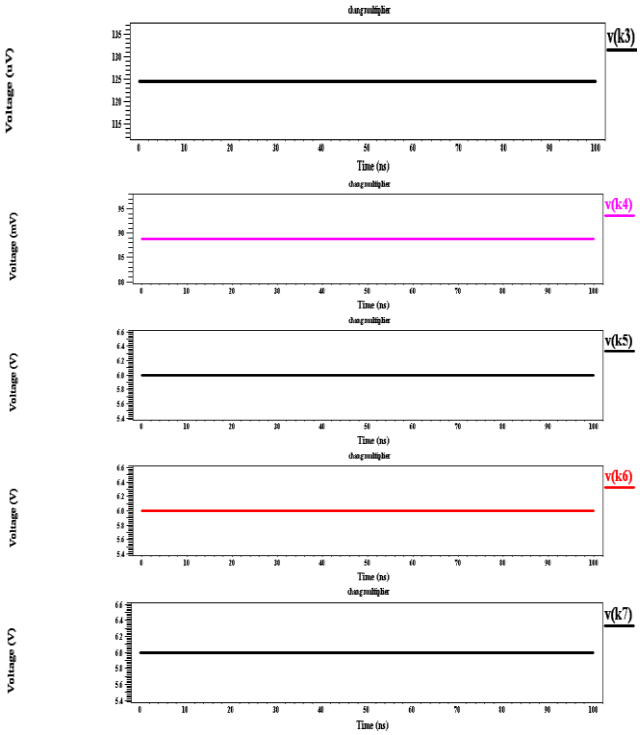


Fig 6: Waveform for Proposed Braun multiplier II

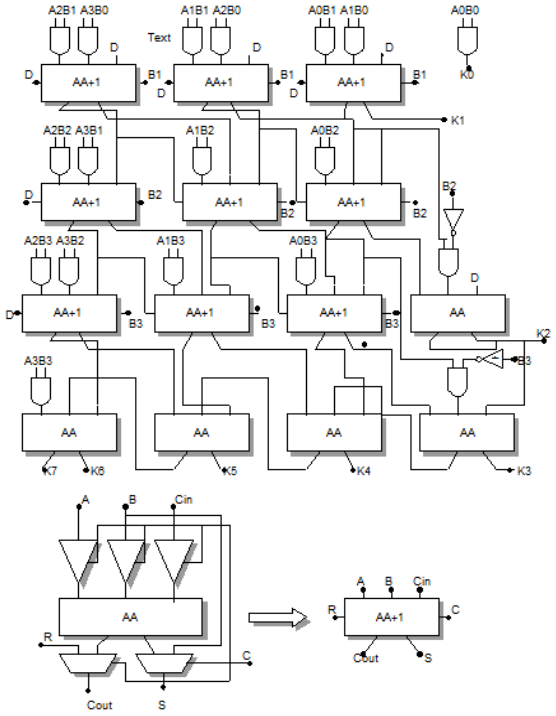


Fig 7: Proposed Braun multiplier III

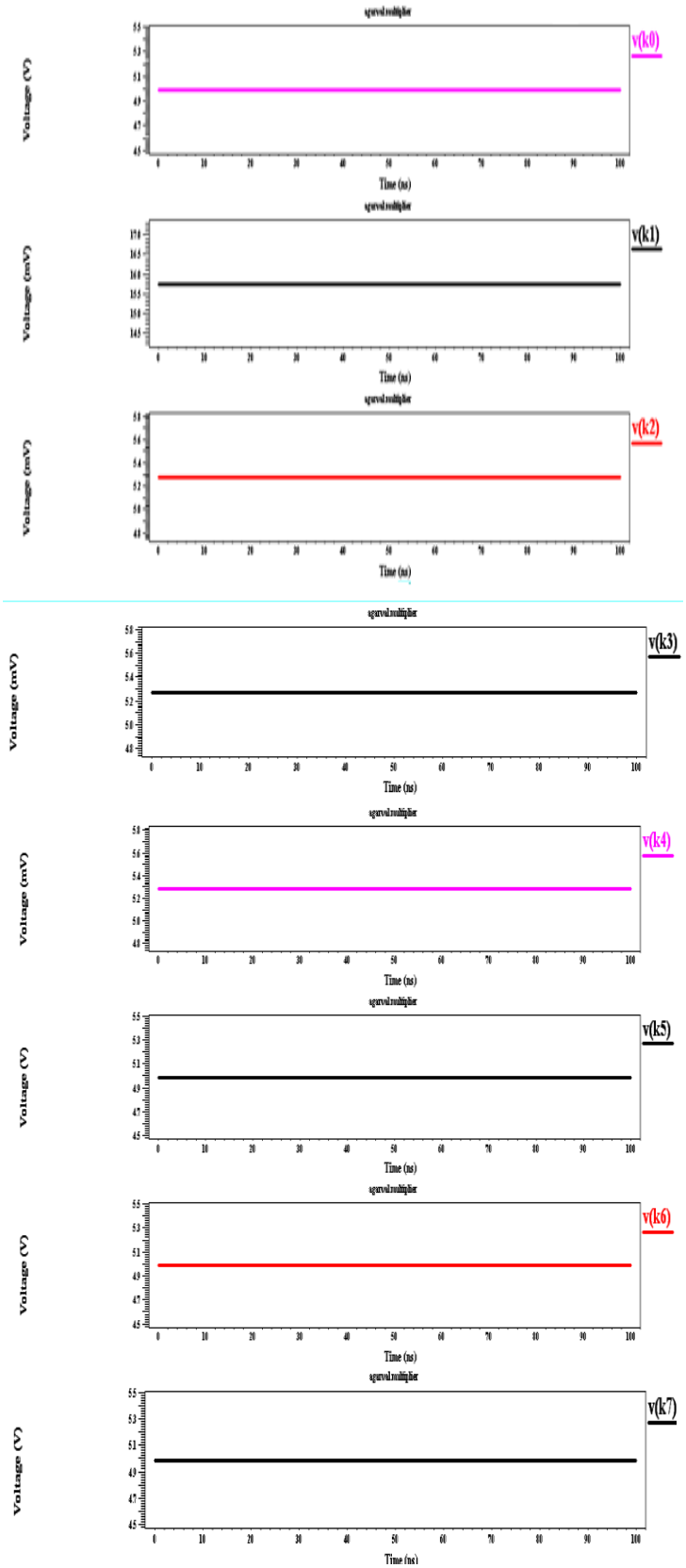


Fig 8: Waveform for Proposed Braun multiplier III

VI. Results and Discussions

The Braun multiplier shown in Figure2 is used with the different adders and the results obtained are listed in table I and table II. Depending on the number of transistors required for designing these multipliers, area is calculated and power consumption for different multipliers are compared in the table II.

Table 1. Area comparison of Multiplier

S.No	Multiplier	No. of transistors
1.	Proposed Braun multiplier I	740
2.	Proposed Braun multiplier II	796
3.	Proposed Braun multiplier III	1020

Table2I. Power comparison of Multiplier

S.No	Multiplier	Maximum power (watts)	Minimum power (watts)	Average power (watts)
1.	Proposed Braun multiplier I	4.172837e-003	4.172837e-003	2.086419e+004
2.	Proposed Braun multiplier II	2.860289e-002	2.860289e-002	1.430145e+005
3.	Proposed Braun multiplier III	1.012971e-004	1.012971e-004	5.064855e+002

VII. Conclusion

This paper, has proposed a methodology to implement a Braun multiplier using different hybrid full adders .The results of Proposed Braun multiplier-I, Proposed Braun multiplier-II and multiplier-III are compared. Power consumption gets reduced when Braun multipliers are designed with different adders like Agarwal adder, Radhakrishnan adder and Chang adder. But for Agarwal adder based Braun multiplier, area is increased when compared to the other Braun multipliers. Thus in CMOS logic, a limitation can be imposed only on one issue. Here power is the factor that is limited with increase in area and time remaining constant

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